IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND-ODESSA DIVISION

REDSTONE LOGICS LLC, ***Plaintiff,***	§	
-v-	§	**7:24-CV-000028-DC-DTG**
NXP SEMICONDUCTORS N.V., NXP B.V., AND NXP USA, INC., ***Defendants.***	§	

CLAIM CONSTRUCTION ORDER

Before the Court are the Parties' claim construction briefs: Defendants NXP Semiconductors N.V., NXP B.V., and NXP USA, Inc.'s Opening Claim Construction Brief (ECF No. 39), Plaintiff Redstone Logics LLC Responsive Claim Construction Brief (ECF No. 41), Defendants' Reply Claim Construction Brief (ECF No. 43), Plaintiff's Sur-Reply Claim Construction Brief (ECF No. 44), and the parties' Joint Claim Construction Statement (ECF No. 45). On February 18, 2025, the Court provided the parties with its Preliminary Claim Constructions, and on February 19, 2025, the Court held a *Markman* hearing. The Court issues this Order to memorialize the Court's final claim construction rulings for the parties, and to inform the parties that the Court will issue a more-detailed Order explaining its analysis in due course. The deadline to file any objections to the undersigned's claim construction rulings (pursuant to Federal Rules of Civil Procedure 59 and 72) does not begin to run until the more-detailed Order is entered on the docket.

I. AGREED CONSTRUCTIONS:

Term No.	Term	Agreed Upon Construction
1	"a first/second set of processor cores" U.S. Patent No. 8,549,339, Claims 1, 21	"a first/second group of two or more processor cores"

II. DISPUTED CONSTRUCTIONS:

Term No.	Term	Redstone's Proposed Construction	NXP's Proposed Construction	Court's Final Construction
1	"the first clock signal is independent from the second clock signal" U.S. Patent No. 8,549,339, Claims 1, 21	Plain and ordinary meaning	Plain and ordinary meaning, where the plain and ordinary meaning requires that the first and second clock signals are provided by or processed (i.e., divided or multiplied) from different reference oscillator clocks.	Plain-and-ordinary meaning, wherein the plain and ordinary meaning does not require that the first and second clock signals depend from different reference oscillator clocks.
2	"each processor core from the first/second set of processor cores is configured to dynamically receive a first/second supply voltage [from a power control block] and a first/second output clock signal" U.S. Patent No. 8,549,339, Claims 1, 21	Plain and ordinary meaning	Indefinite	Not indefinite. Plain-and-ordinary meaning.

3	"located in a periphery of the multi-core processor" U.S. Patent No. 8,549,339, Claim 5	Plain and ordinary meaning	Indefinite	Not indefinite. Plain-and-ordinary meaning.
4	"located in a common region that is substantially central to the first set of processor cores and the second set of processor cores" U.S. Patent No. 8,549,339, Claim 14	Plain and ordinary meaning	Indefinite	Indefinite.

SIGNED this 21st day of February, 2025.

DEREK T. GILLILAND
UNITED STATES MAGISTRATE JUDGE